phoeniX RISC-V Core V0.1

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Preface:

phoeniX is a 5 stage pipelined 32-bit RISC-V processor written in Verilog. This project was started in summer of 2023 in Digital Design Laboratory of Electronics Research Center at Iran University of Science and Technology. This document contains technical specifications and user manual for version 0.1 of phoeniX processor. This version

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